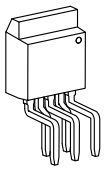
Technical Data

Classification of semiconductor package

SIP
Single In-line Package

A package having leads on a single side of the body.

ZIP
Zigzag In-line Package



A package having Zig-zag formed leads on a single side of the body.

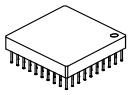
DIP
Dual In-line Package

A package having leads in parallel rows on two opposite sides of the body for through-hole insertion.

SDIP
Shrink DIP

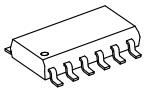
A package which reduced the lead pitch of DIP.

PGA
Pin Grid Array



A package having pins on top or bottom face in a matrix layout of at least three rows and three columns.

SOP
Small Outline Package



A package having gull-wing-shaped leads on two opposite sides of the body.

TSOP
Thin SOP

A package height of SOP exceeds 1.0 mm, and 1.2 mm or less.

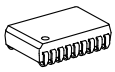
SSOP
Shrink SOP

A package which reduced the lead pitch of SOP.

SON
Small Outline Non-leaded Package

A package having single-inline terminal pads along two opposite edges of the bottom face. The terminal pads may or may not be exposed on the package sides.

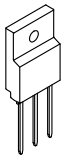
SOJ
Small Outline J-leaded Package



A package having J-shaped leads on two opposite sides of the body.

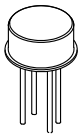
Classification of semiconductor package

TO
Transistor Outline



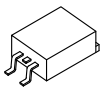
A package that is widely used for transistor, sensors and passive component. And its materials are metal, ceramics and plastics.

CAN Type , Metal Package



Surface Mount Package

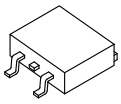
TO-252/D-PAK



A package that enables surface mount soldering by forming leads.

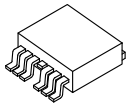
TO-263/D2-PAK

3Pin

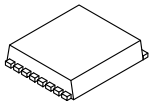


Same as D-PAK, a package that enables surface mount soldering with the lead pitch of 2.54 mm (In case of 3-pin). Number of pins are 3 pins, 5 pins, or 7 pins.

7Pin

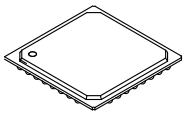


TO-Leadless



Also It is called "TOLL", this package has significantly reduced the mounting area and height, increased the power density, and realized a compact size and high speed.
Used in high current applications such as industrial power supplies.

BGA
Ball Grid Array



A package having balls or bumps on top or bottom face in a matrix of at three rows and three columns or more.

FBGA (CSP)
Fine pitch BGA

A package of BGA having less or equal 0.8mm pitch terminals.

TFBGA
Thin FBGA

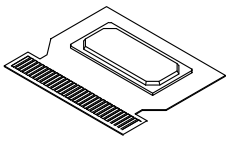
A package height of FBGA exceeds 1.0 mm, and 1.2 mm or less.

VFBGA
Very thin FBGA

A package height of FBGA exceeds 0.8 mm, and 1.0 mm or less.

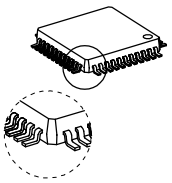
TCP
Tape Carrier Package

A semiconductor package that has the TAB connection and is coated by resin.



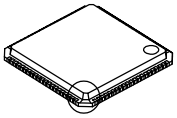
Classification of semiconductor package

QFP
Quad Flat Package

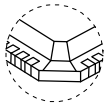


A package having gull-wing-shaped leads on four sides of the body.

QFN
Quad Flat Non-leaded Package



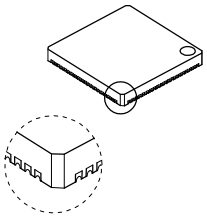
A package having single-inline terminal pads along four edges of the bottom face. The terminal pads may or may not be exposed on the package sides.



CQFN
Ceramic QFN
A name in U.S. is LCC/CLCC.

QFN package having ceramic body.

Wettable Flanks QFN



QFN package with wettable flanks.
This aids in solder wettability on side of packages and in optical inspecting packages such as QFN soldered on a board.

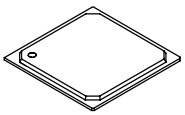
QFJ
Quad Flat J-leaded Package

A package having J-shaped leads on four sides of the body.

PQFJ
Plastic QFJ
A name in U.S. is PLCC.

QFJ package having plastic body.

LGA
Land Grid Array



A package having lands on top or bottom face in a matrix of at least three rows and three columns.

CSP
Chip Size Package

An ultra-compact package that is almost the same size as the built-in semiconductor chip. There are interposer type (BGA, LGA) and lead frame type (LLP, DFN).

Wafer level CSP

CSP that cuts out after wiring processing on the wafer before cutting the die.